An Efficient Method of Measuring in-band Spurious for Wide Band LFM

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Abstract:

Operating frequency band of Radars vary depending on radar's missions. This requirement generates the necessity for selecting spurious free band of operation. Spurious in a desired band of frequency is not known a priori, it can be estimated by practical experiments only. The spurious in the frequency band is a critical parameter considering that it affects SFDR of radar received signal. Wide bandwidth waveform is required for finer resolution. In wideband waveform of high time-bandwidth product it is difficult to figure out the in-band spurious. This paper describes the method of measuring in-band spurious masked under wide band LFM.

Keywords: DDS, FPGA, VHDL, In-band spurious, Linear Frequency Modulation.

I. INTRODUCTION

Radar equipments operate at frequencies close to the concerned band and their spurious emission is a potential source of interference. As the levels of their spurious emissions are specified neither by the manufacturer nor the operator, hence Radars had to be checked by measurements. Advanced Radars requires frequency agile synthesizers which should have good noise performance like phase noise, spurious which makes them suitable for taking the challenges in hostile warfare scenario. The effect of spurious makes even the best imaging Radars crippled in Warfield due to the degraded image quality and false alarms and are more susceptible to jamming.

Spurious is any radio frequency not deliberately created or transmitted, especially in a device which normally does create other frequencies. A harmonic or other signal outside a transmitter's assigned channel would be considered a spurious.

Most modern Radars use Direct Digital Synthesizer (DDS) for generating transmits waveforms. DDS is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. A basic Direct Digital Synthesizer consists of a frequency reference a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC). DDS usually used to gain agility which makes severe tradeoff in spurious performance. DDS spurious sources are Clock Sub Harmonic spurs, Harmonic spurs of output frequency, Phase truncation error, Amplitude truncation error, DAC non linearity and DAC quantization.

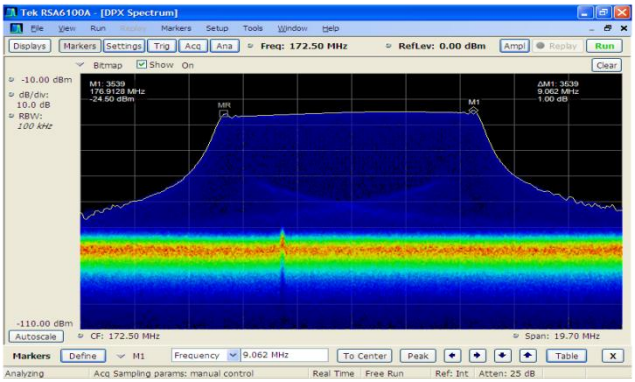

Figure 1: RTSA results showing frequency band in DPX mode.

The paper describes the method of measuring in-band spurious masked under wide band LFM. This was implemented using AD-9858 DDS from Analog Devices. DDS is controlled by writing 32 bit of Control Function register (CFR), Frequency tuning word (FTW), DFTW and 32 bit of DFRRW. Most airborne Radars used for imaging application requires, wide bandwidth transmit and de-chirp waveforms which are generated using DDS. When a wide band LFM is generated for a specific pulse width, it is impossible to measure spurious in the band of interest. Thus to find in-band spurious, a large number of CW spots were generated by applying 32 bit data to FTW register. These data were generated by Matlab programming and saved into block ROM (BROM) and pumped out by the BROM whenever trigger was applied to the BROM. At each rising edge of trigger next location address is pointed and BROM get enabled for the pulse width the trigger. The above described method was implemented using a customized waveform generator card and spurious level was verified through Spectrum Analyzer and Real Time Spectrum Analyzer (RTSA).

II. IMPLEMENTATION SCHEME

The implement method is divided in two parts. First, software implementation is described and later hardware implementation process is explained.

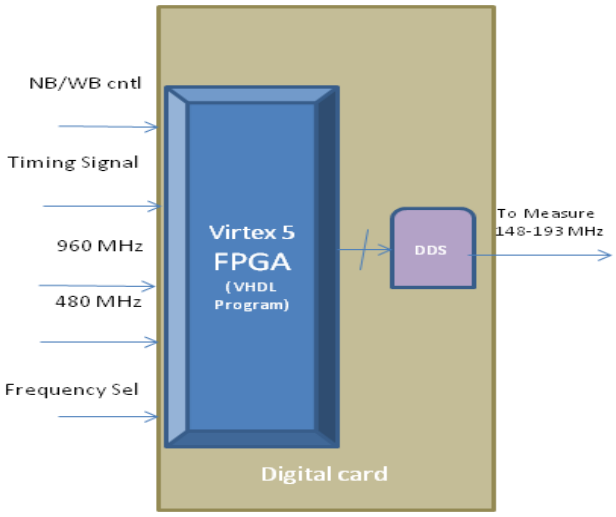

Figure 2: Simplified Implementation Scheme.

The software implementation uses VHDL coding to generate control signals for DDS. The scheme uses Xilinx ISE 12.4 platform. Simulation was completed using ISE simulator and probing of the FPGA signals through Chip-scope Pro 12.4 environment. Timing signals & control signals from RTIO was registered in FPGA. Using these timing and control, Control function registers (CFR) & Frequency tuning word (FTW) was generated. For calculating FTW, following formula is used,

$$FTW = (Fout \times (2) \text{ ^}32)/System\ Clk$$

Where,
FTW = Frequency tuning word,
Fout = Desired output frequency,
System Clk = Clock frequency for DDS, Here it was 960 MHz
Block RAM is used to contain values of FTWs.

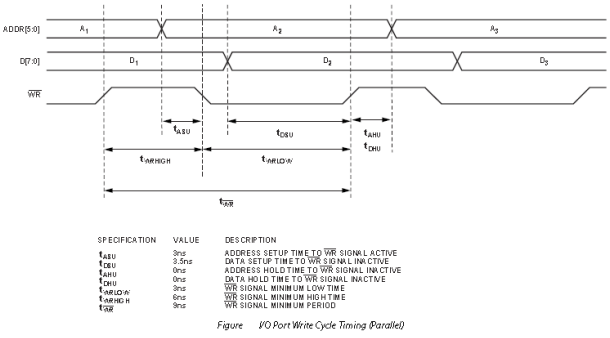

Figure 3: timing diagram for DDS AD 9858.

These FTW values are loaded at each incoming timing pulse. The trigger timing can be set according to measurement time, thus the time period is set to 30 sec which was sufficient for measuring spurious at that spot frequency. Thus in-band spurious measurement was done.
DDS core is provided with reset and enable signal used for synchronization and resetting the initial phase of DDS on pulse to pulse basis. The DDS core is provided with a particular data FTW (Frequency Tuning Word) to generate the carrier frequency. This FTW is of 32 bits, which gives the control information to DDS for generating particular frequency spot through DAC.So for generating slow sweep signals it is required to generate multiple frequency spots. So 6030 frequency spots were generated and saved to BROM core. At each input trigger to DDS, it generates one frequency spots. Hence speed of sweep was controlled and made to 30 sec to measure output on Spectrum Analyser.

III. SIMULATION AND RESOURCE ESTIMATION

The implementation scheme described above is simulated using ISE simulator inbuilt in Xilinx ISE platform. The FPGA Clock period can be set accordingly. Spectrum Analyser is used to compare signal o/p. The Black Box used in the design can be simulated separately using Modelsim simulator. The FPGA resources used by the design can be estimated through resource estimator block. This will provide with an estimation of number of slices, FFs, BROM, LUTs, IOBs required for the design before downloading the design into actual hardware. This result can be compared with post-map actual resource requirement results.

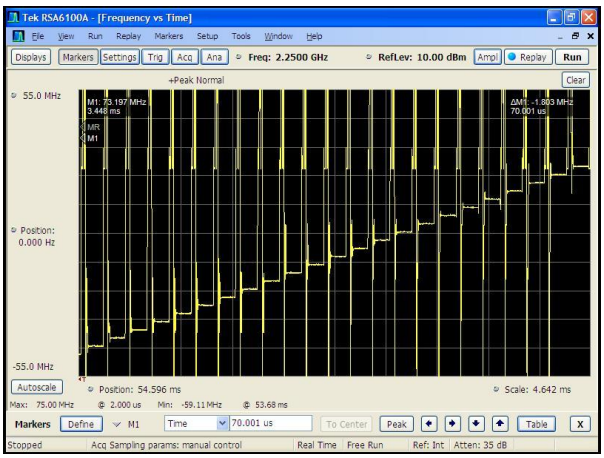

Figure 4: RTSA results showing sweep.

The resource estimation results show around two percent of total FPGA resources are used. So, number of DDS spots can be increased to the maximum number that can be supported by a FPGA. This way resolution can be increased, which is similar to the increasing of the sweep resolution

IV. ADVANTAGES

The effect of spurious makes even the best imaging Radars crippled in Warfield due to the degraded image quality and false alarms and are more susceptible to jamming. In this situation, the current scheme becomes useful to select spurious free spots as well as to know the intensity of spurious and thereby making a decision whether to operate the RADAR at a particular spectrum depending upon hostile situation. This requires no extra hardware and can be implemented in software.

V. CONCLUSION

The in band spurious measurement which was not possible so far without sophisticated instrument is done through a simple method. This truly enhances the test engineer to qualify the RADAR system for its efficiency over design goals like image quality, ECCM, jamming resistance.

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Nitesh Kumar received his B. tech degree in Electronics and Communication Engineering from National Institute of Technology Durgapur (W.B.) in 2007. Since 2008, he has been working in LRDE, DRDO, Bangalore and has contributed in the area of Exciter, Digital Receiver and Digital Waveform Generation. He has worked in Weapon Locating Radar and currently he is working for the Active Electronically Scanned Array Radar (AESA) for the LCA.

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